19-4782; Rev 2; 9/04

EVALUATION KIT AVAILABLE

Multirange, +5V, 8-Channel, Serial 12-Bit ADCs

MAX1270/MAX1271

General Description

The MAX1270/MAX1271 are multirange, 12-bit data-acquisition systems (DAS) that require only a single +5V supply for operation, yet accept signals at their analog inputs that can span above the power-supply rail and below ground. These systems provide eight analog input channels that are independently software programmable for a variety of ranges: ±10V, ±5V, 0 to +10V, 0 to +5V for the MAX1270; $\pm V_{REF}$, $\pm V_{REF}/2$, 0 to V_{REF}, 0 to $V_{REF}/2$ for the MAX1271. This range switching increases the effective dynamic range to 14 bits and provides the flexibility to interface 4–20mA, ±12V, and ±15V powered sensors directly to a single +5V system. In addition, these converters are fault protected to ±16.5V; a fault condition on any channel will **not** affect the conversion result of the selected channel. Other features include a 5MHz bandwidth track/hold, software-selectable internal/external clock, 110ksps throughput rate, and internal 4.096V or external reference operation.

The MAX1270/MAX1271 serial interface directly connects to SPI™/QSPI™ and MICROWIRE™ devices without external logic.

A hardware shutdown input ($\overline{SHDN}$) and two software-programmable power-down modes, standby (STBYPD) or full power-down (FULLPD), are provided for low-current shutdown between conversions. In standby mode, the reference buffer remains active, eliminating startup delays.

The MAX1270/MAX1271 are available in 24-pin narrow PDIP or space-saving 28-pin SSOP packages.

Applications

Industrial Control Systems
Data-Acquisition Systems
Battery-Powered Instruments
Automatic Testing
Robotics
Medical Instruments

Ordering Information

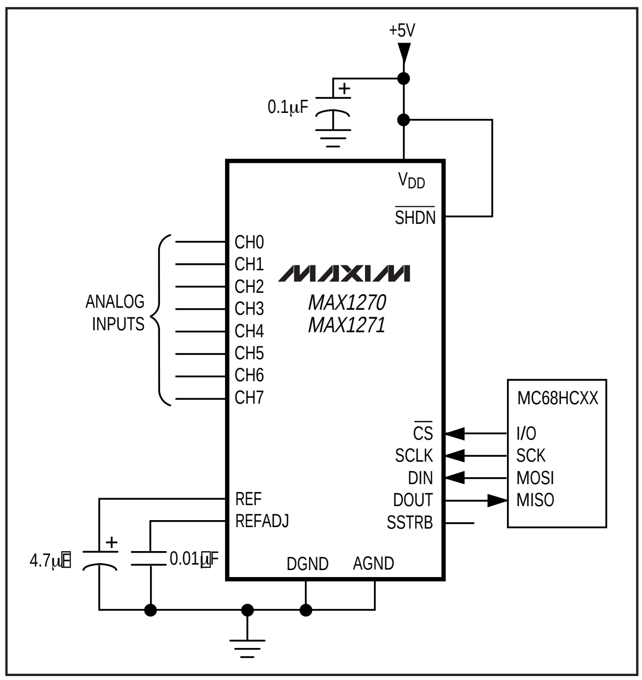
PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX1270ACNG	0°C to +70°C	24 Narrow PDIP	±0.5
MAX1270BCNG	0°C to +70°C	24 Narrow PDIP	±1
MAX1270ACAI	0°C to +70°C	28 SSOP	±0.5
MAX1270BCAI	0°C to +70°C	28 SSOP	±1

Ordering Information continued at end of data sheet.

Features

- ♦ 12-Bit Resolution, 0.5 LSB Linearity
- ♦ +5V Single-Supply Operation
- ♦ SPI/QSPI and MICROWIRE-Compatible 3-Wire Interface
- ♦ Four Software-Selectable Input Ranges
  MAX1270: 0 to +10V, 0 to +5V, ±10V, ±5V
  MAX1271: 0 to V_{REF}, 0 to $V_{REF}/2$, $\pm V_{REF}$, $\pm V_{REF}/2$
- ♦ Eight Analog Input Channels
- ♦ 110ksps Sampling Rate
- ♦ ±16.5V Overvoltage-Tolerant Input Multiplexer
- ♦ Internal 4.096V or External Reference
- ♦ Two Power-Down Modes
- ♦ Internal or External Clock
- ♦ 24-Pin Narrow PDIP or 28-Pin SSOP Packages

Typical Operating Circuit



Pin Configurations appear at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND..-0.3V to +6V
AGND to DGND...-0.3V to +0.3V
CH0–CH7 to AGND .... ±16.5V
REF, REFADJ to AGND ....-0.3V to (V_{DD} + 0.3V)
SSTRB, DOUT to DGND.............................-0.3V to (V_{DD} + 0.3V)
$\overline{SHDN}$, $\overline{CS}$, DIN, SCLK to DGND..............................-0.3V to +6V
Max Current into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
24-Pin Narrow DIP (derate 13.33mW/°C above +70°C)..1067mW
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW

Operating Temperature Ranges
MAX127_C_ _..0°C to +70°C
MAX127_E_ _..-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5.0V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = +4.096V; 4.7µF at REF; external clock; f_{CLK} = 2.0MHz, 50% duty cycle (MAX127_B); f_{CLK} = 1.8MHz, 50% duty cycle (MAX127_A); 18 clock/conversion cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution				12			Bits
Integral Nonlinearity	INL	MAX127_A				±0.5	LSB
		MAX127_B				±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature				±1	LSB
Offset Error		Unipolar	MAX127_A			±3	LSB
			MAX127_B			±5	
		Bipolar	MAX127_A			±5	
			MAX127_B			±10	
Channel-to-Channel Offset Error Matching		Unipolar			±0.1		LSB
		Bipolar			±0.3		
Gain Error (Note 2)		Unipolar	MAX127_A			±7	LSB
			MAX127_B			±10	
		Bipolar	MAX127_A			±7	
			MAX127_B			±10	
Gain Error Temperature Coefficient (Note 2)		Unipolar, external reference			±3		ppm/°C
		Bipolar, external reference			±5		
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, ±10V_{P-P} (MAX1270), or ±4.096V_{P-P} (MAX1271), f_{SAMPLE} = 110ksps (MAX127_B), f_{SAMPLE} = 100ksps (MAX127_A))							
Signal-to-Noise + Distortion Ratio	SINAD			70			dB
Total Harmonic Distortion	THD	Up to the 5th harmonic			-87	-78	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		50kHz (Note 3)			-86		dB
		DC, V_{IN} = ±16.5V			-96		
Aperture Delay		External clock mode			15		ns
Aperture Jitter		External clock mode			<50		ps
		Internal clock mode			10		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5.0V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = +4.096V; 4.7µF at REF; external clock; f_{CLK} = 2.0MHz, 50% duty cycle (MAX127_B); f_{CLK} = 1.8MHz, 50% duty cycle (MAX127_A); 18 clock/conversion cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG INPUT								
Track/Hold Acquisition Time	t_{ACQ}	MAX127_A, f_{CLK} = 1.8MHz					3.3	µs
		MAX127_B, f_{CLK} = 2.0MHz					3.0	
Small-Signal Bandwidth		-3dB rolloff	±10V or ±V_{REF} range			5		MHz
			±5V or ±V_{REF}/2 range			2.5		
			0 to 10V or 0 to V_{REF} range			2.5		
			0 to 5V or 0 to V_{REF}/2 range			1.25		
Input Voltage Range (Table 3)	V_{IN}	Unipolar (BIP = 0), Table 3	MAX1270	RNG = 1	0		10	V
				RNG = 0	0		5	
			MAX1271	RNG = 1	0		V_{REF}	
				RNG = 0	0		V_{REF}/2	
		Bipolar (BIP = 1), Table 3	MAX1270	RNG = 1	-10		+10	
				RNG = 0	-5		+5	
			MAX1271	RNG = 1	-V_{REF}		+V_{REF}	
				RNG = 0	-V_{REF}/2		+V_{REF}/2	
Input Current	I_{IN}	Unipolar	MAX1270	0 to 10V range	-10		+720	µA
				0 to 5V range	-10		+360	
			MAX1271		-10	0.1	+10	
		Bipolar	MAX1270	±10V range	-1200		+720	
				±5V range	-600		+360	
			MAX1271	±V_{REF} range	-1200		+10	
				±V_{REF}/2 range	-600		+10	
Dynamic Resistance	$\Delta V_{IN}/\Delta I_{IN}$	Unipolar				21		kΩ
		Bipolar				16		
Input Capacitance		(Note 4)					40	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5.0V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = +4.096V; 4.7µF at REF; external clock; f_{CLK} = 2.0MHz, 50% duty cycle (MAX127_B); f_{CLK} = 1.8MHz, 50% duty cycle (MAX127_A); 18 clock/conversion cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERNAL REFERENCE							
REF Output Voltage	V_{REF}	T_A = +25°C		4.076	4.096	4.116	V
REF Output Tempco	TC V_{REF}	MAX1270_C/MAX1271_C			±15		ppm/°C
		MAX1270_E/MAX1271_E			±30		
Output Short-Circuit Current					30		mA
Load Regulation		0 to 0.5mA output current (Note 5)				10	mV
Capacitive Bypass at REF				4.7			µF
Capacitive Bypass at REFADJ				0.01			µF
REFADJ Output Voltage				2.465	2.500	2.535	V
REFADJ Adjustment Range		Figure 1			±1.5		%
Buffer Voltage Gain					1.638		V/V
REFERENCE INPUT (Reference buffer disabled, reference input applied to REF)							
Input Voltage Range				2.40		4.18	V
Input Current		V_{REF} = 4.18V	Normal or STBYPD			400	µA
			FULLPD			1	
Input Resistance		V_{REF} = 4.18V	Normal or STBYPD	10			kΩ
			FULLPD	4.18			MΩ
REFADJ Threshold for Buffer Disable				V_{DD} - 0.5			V
POWER REQUIREMENT							
Supply Voltage	V_{DD}			4.75		5.25	V
Supply Current	I_{DD}	Normal	Bipolar range			18	mA
			Unipolar range		6	10	
		STBYPD power-down mode (Note 6)			700	850	µA
		FULLPD power-down mode			120	220	
Power-Supply Rejection Ratio (Note 7)	PSRR	External reference = 4.096V			±0.1	±0.5	LSB
		Internal reference			±0.5		
TIMING							
External Clock Frequency Range	f_{SCLK}	MAX127_A		0.1		1.8	MHz
		MAX127_B		0.1		2.0	
Acquisition Phase		External clock mode (Note 8)	MAX127_A	3.3			µs
			MAX127_B	3.0			
		Internal clock mode, Figure 9		3		5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5.0V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = +4.096V; 4.7µF at REF; external clock; f_{CLK} = 2.0MHz, 50% duty cycle (MAX127_B); f_{CLK} = 1.8MHz, 50% duty cycle (MAX127_A); 18 clock/conversion cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Time	t_{CONV}	External clock mode (Note 8)	MAX127_A	6.6			µs
			MAX127_B	6.0			
		Internal clock mode, Figure 9		6	7.7	11	
Throughput Rate		External clock mode	MAX127_A			100	ksps
			MAX127_B			110	
		Internal clock mode				43	
Bandgap Reference Startup Time		Power-up (Note 9)			200		µs
Reference Buffer Settling Time		To 0.1mV, REF bypass capacitor fully discharged	C_{REF} = 4.7µF		8		ms
			C_{REF} = 33µF		60		
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, and $\overline{SHDN}$)							
Input High Threshold Voltage	V_{IH}					2.4	V
Input Low Threshold Voltage	V_{IL}			0.8			V
Input Hysteresis	V_{HYS}				0.2		V
Input Leakage Current	I_{IN}	V_{IN} = 0 to V_{DD}		-10		+10	µA
Input Capacitance	C_{IN}	(Note 4)				15	pF
DIGITAL OUTPUTS (DOUT, SSTRB)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA			0.4		
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD} - 0.5			V
Tri-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}		-10		+10	µA
Tri-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 4)				15	pF

Multirange, +5V, 8-Channel, Serial 12-Bit ADCs

TIMING CHARACTERISTICS

(V_{DD} = +4.75V to +5.25V; unipolar/bipolar range; external reference mode, V_{REF} = +4.096V; 4.7µF at REF; external clock; f_{CLK} = 2.0MHz (MAX127_B); f_{CLK} = 1.8MHz (MAX127_A); T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.) (Figures 2, 5, 7, 10)

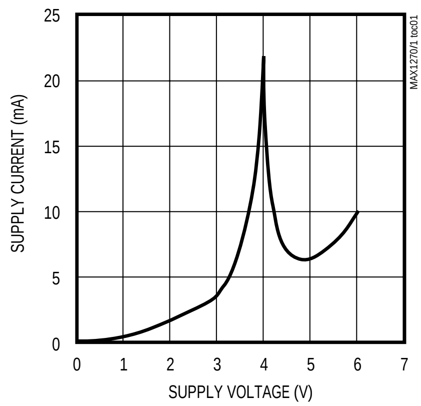
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIN to SCLK Setup	t_{DS}		100			ns
DIN to SCLK Hold	t_{DH}				0	ns
SCLK Fall to Output Data Valid	t_{DO}		20		170	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF			120	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF			100	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
SCLK Pulse-Width High	t_{CH}		200			ns
SCLK Pulse-Width Low	t_{CL}		200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF			200	ns
$\overline{CS}$ to SSTRB Output Enable	t_{SDV}	C_{LOAD} = 100pF, external clock mode only			200	ns
$\overline{CS}$ to SSTRB Output Disable	t_{STR}	C_{LOAD} = 100pF, external clock mode only			200	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 4)	0			ns

Note 1: Accuracy specifications tested at V_{DD} = +5.0V. Performance at power-supply tolerance limit is guaranteed by power-supply rejection test.
Note 2: External reference: V_{REF} = 4.096V, offset error nulled. Ideal last-code transition = FS - 3/2 LSB.
Note 3: Ground "on" channel; sine wave applied to all "off" channels. V_{IN} = ±5V (MAX1270), V_{IN} = ±4V (MAX1271).
Note 4: Guaranteed by design, not production tested.
Note 5: Use static external loads during conversion for specified accuracy.
Note 6: Tested using internal reference.
Note 7: PSRR measured at full scale. Tested for the ±10V (MAX1270) and ±4.096V (MAX1271) input ranges.
Note 8: Acquisition phase and conversion time are dependent on the clock period; clock has 50% duty cycle (Figure 6).
Note 9: Not production tested. Provided for design guidance only.

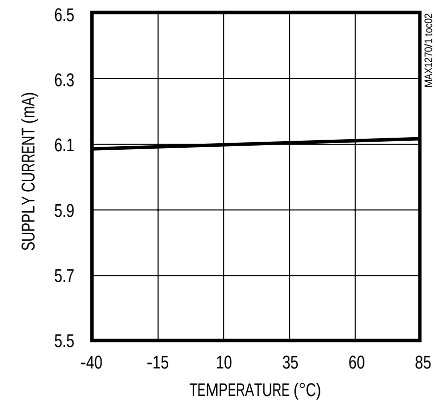
Typical Operating Characteristics

(Typical Operating Circuit, V_{DD} = +5V; external reference mode, V_{REF} = +4.096V; 4.7µF at REF; external clock, f_{CLK} = 2MHz; 110ksps; T_A = +25°C, unless otherwise noted.)

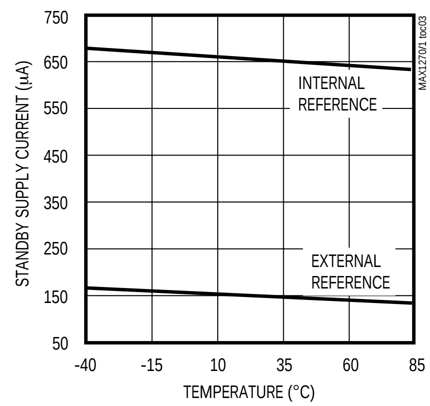
SUPPLY CURRENT vs. SUPPLY VOLTAGE



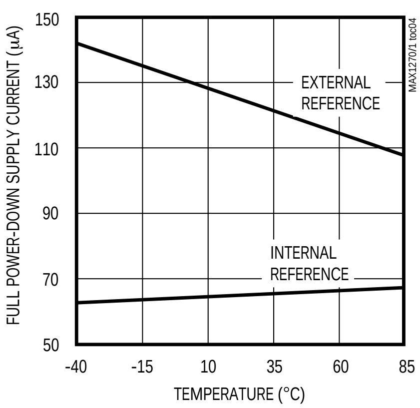
SUPPLY CURRENT vs. TEMPERATURE



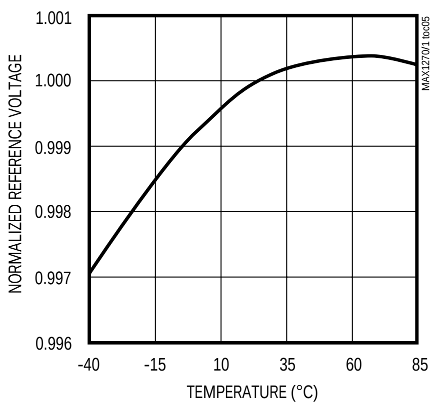
STANDBY SUPPLY CURRENT vs. TEMPERATURE



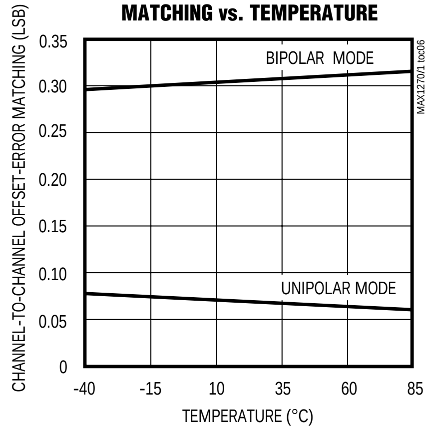
FULL POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



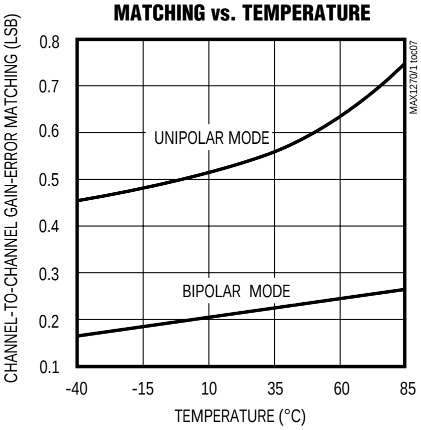
NORMALIZED REFERENCE VOLTAGE vs. TEMPERATURE



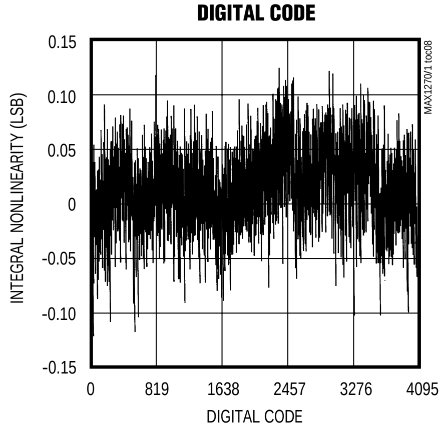
CHANNEL-TO-CHANNEL OFFSET-ERROR MATCHING vs. TEMPERATURE



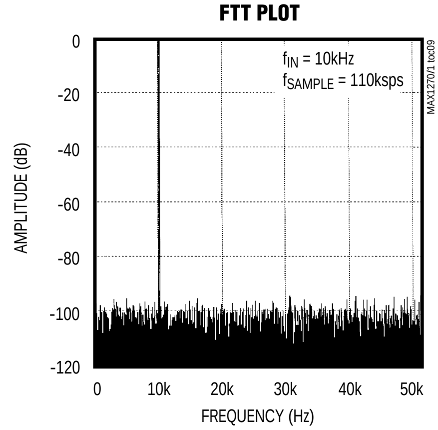
CHANNEL-TO-CHANNEL GAIN-ERROR MATCHING vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. DIGITAL CODE



FTT PLOT

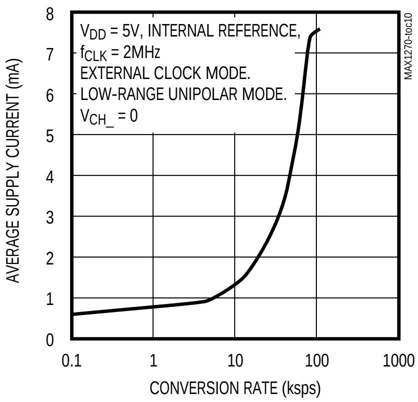


Multirange, +5V, 8-Channel, Serial 12-Bit ADCs

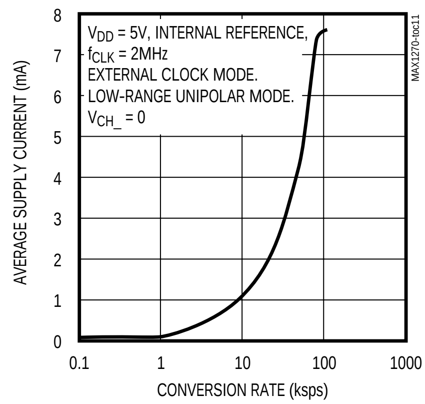
Typical Operating Characteristics (continued)

(Typical Operating Circuit, V_{DD} = +5V; external reference mode, V_{REF} = +4.096V; 4.7µF at REF; external clock, f_{CLK} = 2MHz; 110ksps; T_A = +25°C, unless otherwise noted.)

AVERAGE SUPPLY CURRENT vs. CONVERSION RATE (USING STANDBY)



AVERAGE SUPPLY CURRENT vs. CONVERSION RATE (USING FULLPD)



Pin Description

PIN		NAME	FUNCTION
PDIP	SSOP		
1	1	V_{DD}	+5V Supply. Bypass with a 0.1µF capacitor to AGND.
2, 4	2, 3	DGND	Digital Ground
3, 9, 22, 24	4, 7, 8, 11, 22, 24, 25, 28	N.C.	No Connection. No internal connection.
5	5	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed.
6	6	$\overline{CS}$	Active-Low Chip-Select Input. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
7	9	DIN	Serial Data Input. Data is clocked in on the rising edge of SCLK.
8	10	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low after the falling edge of the eighth SCLK and returns high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high in external clock mode.
10	12	DOUT	Serial Data Output. Data is clocked out on the falling edge of SCLK. High impedance when $\overline{CS}$ is high.
11	13	$\overline{SHDN}$	Shutdown Input. When low, device is in FULLPD mode. Connect high for normal operation.
12	14	AGND	Analog Ground
13–20	15–21, 23	CH0–CH7	Analog Input Channels
21	26	REFADJ	Bandgap Voltage-Reference Output/External Adjust Pin. Bypass with a 0.01µF capacitor to AGND. Connect to V_{DD} when using an external reference at REF.
23	27	REF	Reference-Buffer Output/ADC Reference Input. In internal reference mode, the reference buffer provides a 4.096V nominal output, externally adjustable to REFADJ. In external reference mode, disable the internal reference by pulling REFADJ to V_{DD} and applying the external reference to REF.

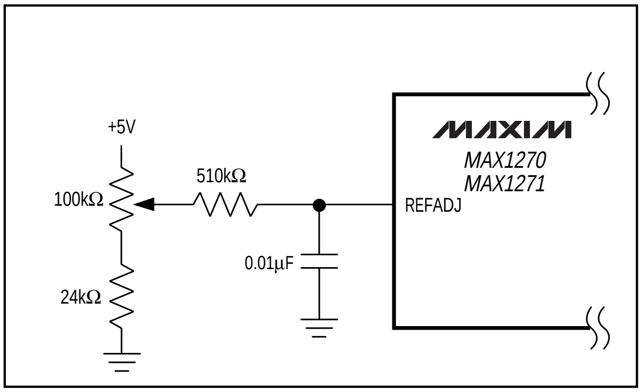


Figure 1. Reference-Adjust Circuit

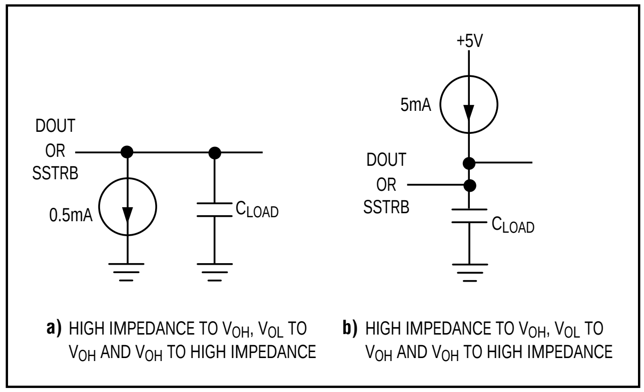


Figure 2. Output Load Circuit for Timing Characteristics

Detailed Description

Converter Operation

The MAX1270/MAX1271 multirange, fault-tolerant ADCs use successive approximation and internal track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. Figure 3 shows the block diagram of the MAX1270/MAX1271.

Analog-Input Track/Hold

The T/H enters tracking/acquisition mode on the falling edge of the sixth clock in the 8-bit input control word, and enters hold/conversion mode when the timed acquisition interval (six clock cycles, 3µs minimum) ends. In internal clock mode, the acquisition is timed by two external clock cycles and four internal clock cycles.

When operating in bipolar (MAX1270 and MAX1271) or unipolar mode (MAX1270) the signal applied at the input channel is rescaled through the resistor-divider network formed by R1, R2, and R3 (Figure 4); a low impedance (<4Ω) input source is recommended to minimize gain error. When the MAX1271 is configured for unipolar mode, the channel input resistance (R_{IN}) becomes a fixed 5.12kΩ (typ). Source impedances below 15kΩ (0 to V_{REF}) and 5kΩ (0 to V_{REF}/2) do not significantly affect the AC performance of the ADC.

The acquisition time (t_{ACQ}) is a function of the source output resistance, the channel input resistance, and the T/H capacitance. Higher source impedances can be used if an input capacitor is connected between the analog inputs and AGND. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

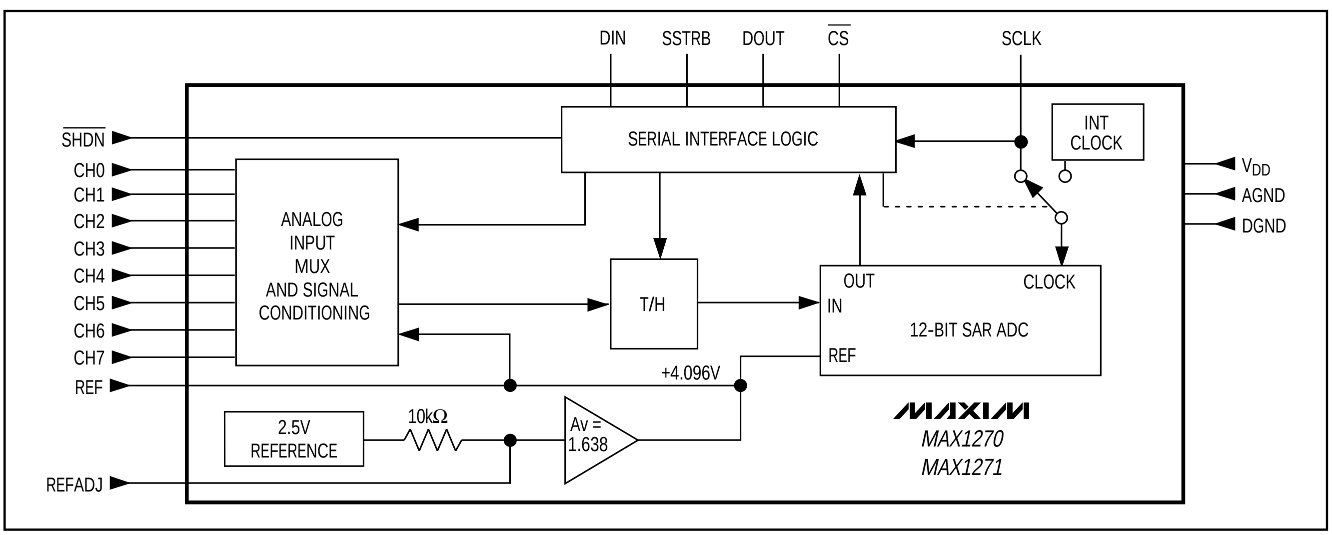


Figure 3. Block Diagram

Input Bandwidth

The ADC's input small-signal bandwidth depends on the selected input range and varies from 1.5MHz to 5MHz (see *Electrical Characteristics*). The MAX1270B/MAX1271B maximum sampling rate is 110ksps (100ksps for the MAX1270A/MAX1271A). By using undersampling techniques, it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate.

To avoid high-frequency signals being aliased into the frequency band of interest, anti-aliasing filtering is recommended.

Input Range and Protection

The MAX1270/MAX1271 have software-selectable input ranges. Each analog input channel can be independently programmed to one of four ranges by setting the appropriate control bits (RNG, BIP) in the control byte (Table 1). The MAX1270 has selectable input ranges extending to ±10V (±V_{REF} x 2.441), while the MAX1271 has selectable input ranges extending to ±V_{REF}. Figure 4 shows the equivalent input circuit.

A resistor network on each analog input provides ±16.5V fault protection for all channels. Whether or not the channel is on, this circuit limits the current going into or out of the pin to less than 2mA. This provides an added layer of protection when momentary overvoltages occur at the selected input channel, when a negative signal is applied to the input, and when the device is configured for unipolar mode. The overvoltage protection is active even if the device is in power-down mode or if V_{DD} = 0.

Digital Interface

The MAX1270/MAX1271 feature a serial interface that is fully compatible with SPI/QSPI and MICROWIRE devices. For SPI/QSPI, set CPOL = 0, CPHA = 0 in the SPI control registers of the microcontroller. Figure 5 shows detailed serial-interface timing information. See Table 1 for details on programming the input control byte.

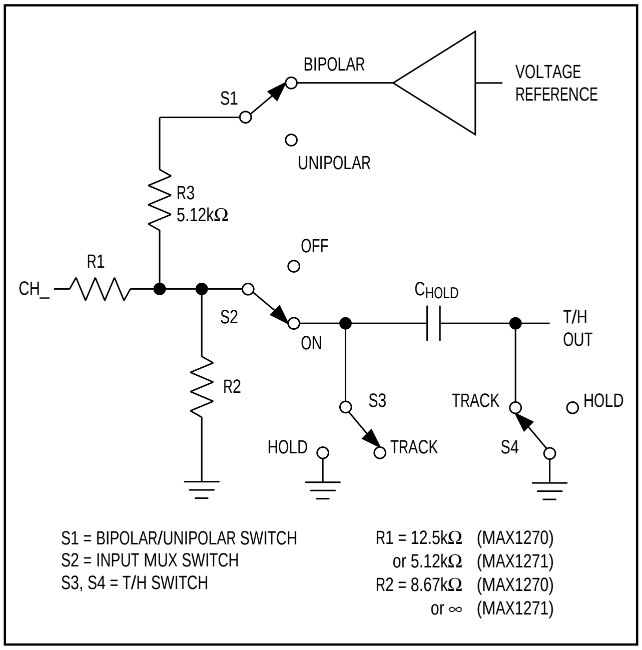


Figure 4. Equivalent Input Circuit

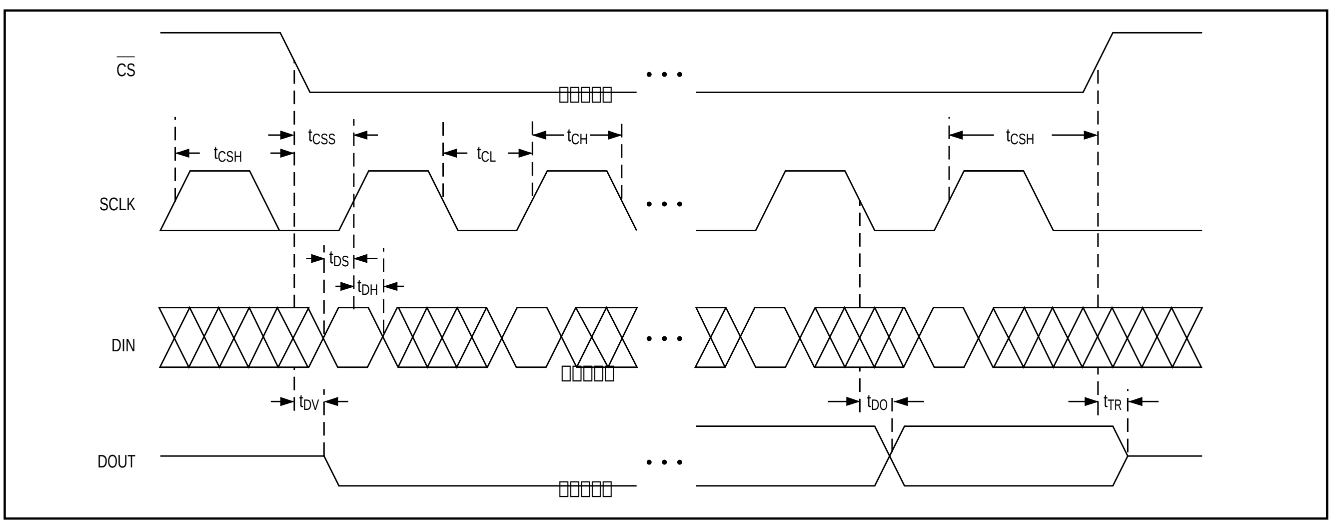


Figure 5. Detailed Serial-Interface Timing

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	RNG	BIP	PD1	PD0

BIT	NAME	DESCRIPTION
7 (MSB)	START	First logic 1 after $\overline{CS}$ goes low defines the beginning of the control byte.
6, 5, 4	SEL2, SEL1, SEL0	These 3 bits select the desired “on” channel (Table 2).
3	RNG	Selects the full-scale input voltage range (Table 3).
2	BIP	Selects the unipolar or bipolar conversion mode (Table 3).
1, 0 (LSB)	PD1, PD0	Select clock and power-down modes (Table 4).

Table 2. Channel Selection

SEL2	SEL1	SEL0	CHANNEL
0	0	0	CH0
0	0	1	CH1
0	1	0	CH2
0	1	1	CH3
1	0	0	CH4
1	0	1	CH5
1	1	0	CH6
1	1	1	CH7

Table 4. Power-Down and Clock Selection

PD1	PD0	MODE
0	0	Normal operation (always on), internal clock mode.
0	1	Normal operation (always on), external clock mode.
1	0	Standby power-down mode (STBYPD), clock mode unaffected.
1	1	Full power-down mode (FULLPD), clock mode unaffected.

Table 3. Range and Polarity Selection for MAX1270/MAX1271

RANGE AND POLARITY SELECTION FOR THE MAX1270					
INPUT RANGE	**RNG**	**BIP**	**Negative FULL SCALE**	**ZERO SCALE (V)**	**FULL SCALE**
0 to +5V	0	0	—	0	V_{REF} x 1.2207
0 to +10V	1	0	—	0	V_{REF} x 2.4414
±5V	0	1	$-V_{REF}$ x 1.2207	0	V_{REF} x 1.2207
±10V	1	1	$-V_{REF}$ x 2.4414	0	V_{REF} x 2.4414
RANGE AND POLARITY SELECTION FOR THE MAX1271					
INPUT RANGE	**RNG**	**BIP**	**Negative FULL SCALE**	**ZERO SCALE (V)**	**FULL SCALE**
0 to $V_{REF}/2$	0	0	—	0	$V_{REF}/2$
0 to V_{REF}	1	0	—	0	V_{REF}
$\pm V_{REF}/2$	0	1	$-V_{REF}/2$	0	$V_{REF}/2$
$\pm V_{REF}$	1	1	$-V_{REF}$	0	V_{REF}

Input Data Format

Input data (control byte) is clocked in at DIN at the rising edge of SCLK. $\overline{CS}$ enables communication with the MAX1270/MAX1271. After $\overline{CS}$ falls, the first arriving logic 1 bit represents the start bit (MSB) of the input control byte. The start bit is defined as:

> The first high bit clocked into DIN with $\overline{CS}$ low anytime the converter is idle; e.g., after V_{DD} is applied.
>
> OR
>
> The first high bit clocked into DIN after bit 6 (D6) of a conversion in progress is clocked onto DOUT.

Output Data Format

Output data is clocked out on the falling edge of SCLK at DOUT, MSB first (D11). In unipolar mode, the output is straight binary. For bipolar mode, the output is two's complement binary. For output binary codes, refer to the *Transfer Function* section.

How to Start a Conversion

The MAX1270/MAX1271 use either an external serial clock or the internal clock to complete an acquisition and perform a conversion. In both clock modes, the external clock shifts data in and out. See Table 4 for details on programming clock modes.

The falling edge of $\overline{CS}$ does not start a conversion on the MAX1270/MAX1271; a control byte is required for each conversion. Acquisition starts after the sixth bit is programmed in the input control byte. Conversion starts when the acquisition time, six clock cycles, expires.

Keep $\overline{CS}$ low during successive conversions. If a start-bit is received after $\overline{CS}$ transitions from high to low, but before the output bit 6 (D6) becomes available, the current conversion will terminate and a new conversion will begin.

External Clock Mode (PD1 = 0, PD0 = 1)

In external clock mode, the clock shifts data in and out of the MAX1270/MAX1271 and controls the acquisition and conversion timings. When acquisition is done, SSTRB pulses high for one clock cycle and conversion begins. Successive-approximation bit decisions appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). Additional SCLK falling edges will result in zeros appearing at DOUT. Figure 7 shows the SSTRB timing in external clock mode.

SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB and DOUT will output a logic low.

The conversion must be completed in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the clock period exceeds 10µs, or if serial-clock interruptions could cause the conversion interval to exceed 120µs. The fastest the MAX1270/MAX1271 can run is 18 clocks per conversion in external clock mode, and with a clock rate of 2MHz, the maximum sampling rate is 111 ksps (Figure 8). In order to achieve maximum throughput, keep $\overline{CS}$ low, use external clock mode with a continuous SCLK, and start the following control byte after bit 6 (D6) of the conversion in progress is clocked onto DOUT.

If $\overline{CS}$ is low and SCLK is continuous, guarantee a start bit by first clocking in 18 zeros.

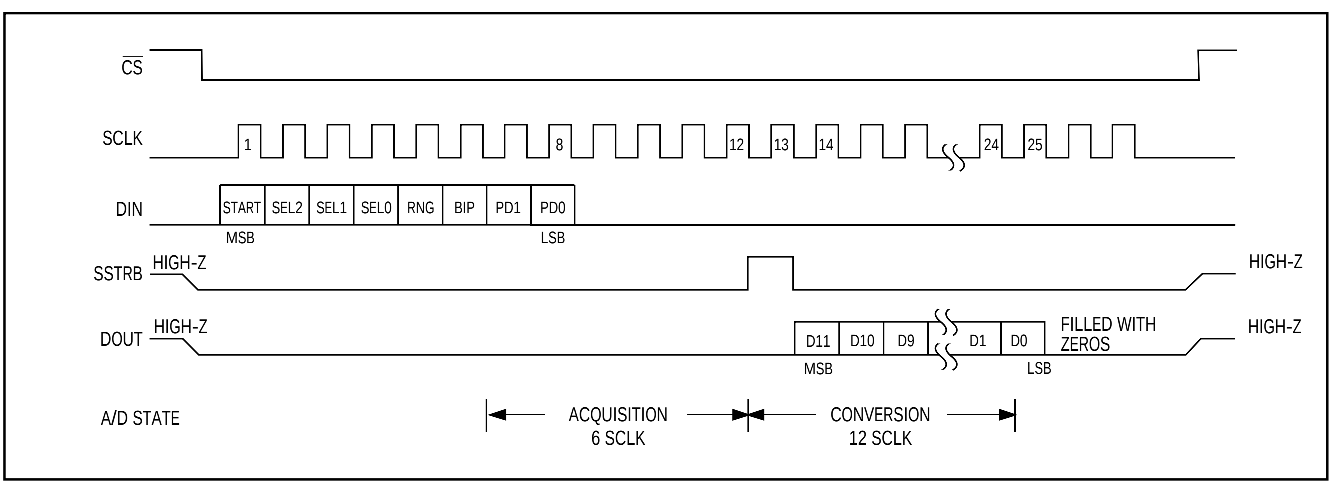


Figure 6. External Clock Mode—25 Clocks/Conversion Timing

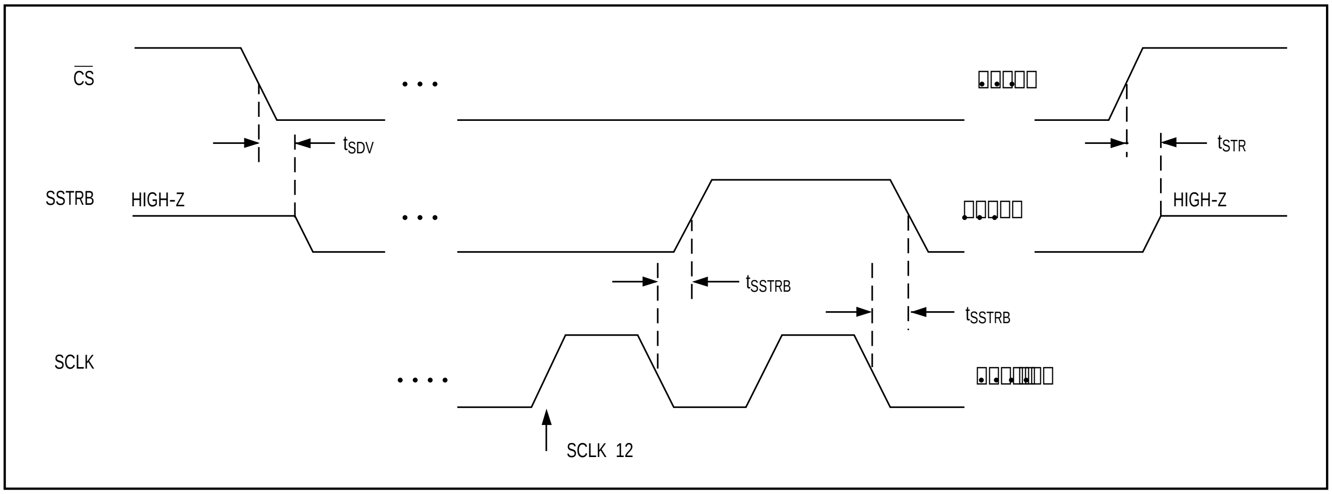


Figure 7. External Clock Mode—SSTRB Detailed Timing

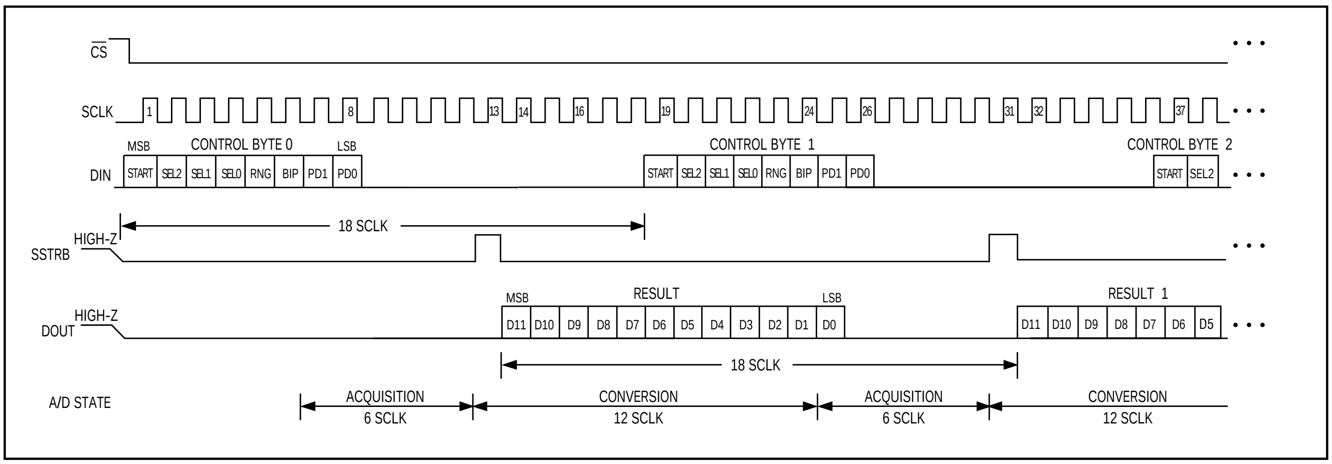


Figure 8. External Clock Mode—18 Clocks/Conversion Timing

Internal Clock Mode (PD1 = 0, PD0 = 0)

In internal clock mode, the MAX1270/MAX1271 generate their conversion clock internally. This frees the microprocessor from the burden of running the acquisition and the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate from 0 to typically 10MHz.

SSTRB goes low after the falling edge of the last bit (PD0) of the control byte has been shifted in, and returns high when the conversion is complete. Acquisition is completed and conversion begins on the falling edge of the 4th internal clock pulse after the control byte; conversion ends on the falling edge of the 16th internal clock pulse (12 internal clock cycle pulses are used for conversion). SSTRB will remain low for a maximum of 15µs, during which time SCLK should remain low for best noise performance. An internal register stores data while the conversion is in progress. The MSB of the result byte (D11) is present at DOUT starting at the falling edge of the last internal clock of conversion. Successive falling edges of SCLK will shift the remaining data out of this register (Figure 9). Additional SCLK edges will result in zeros on DOUT.

When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high. Pulling $\overline{CS}$ high prevents data from being clocked in and tri-states DOUT, but does not adversely affect a

Multirange, +5V, 8-Channel, Serial 12-Bit ADCs

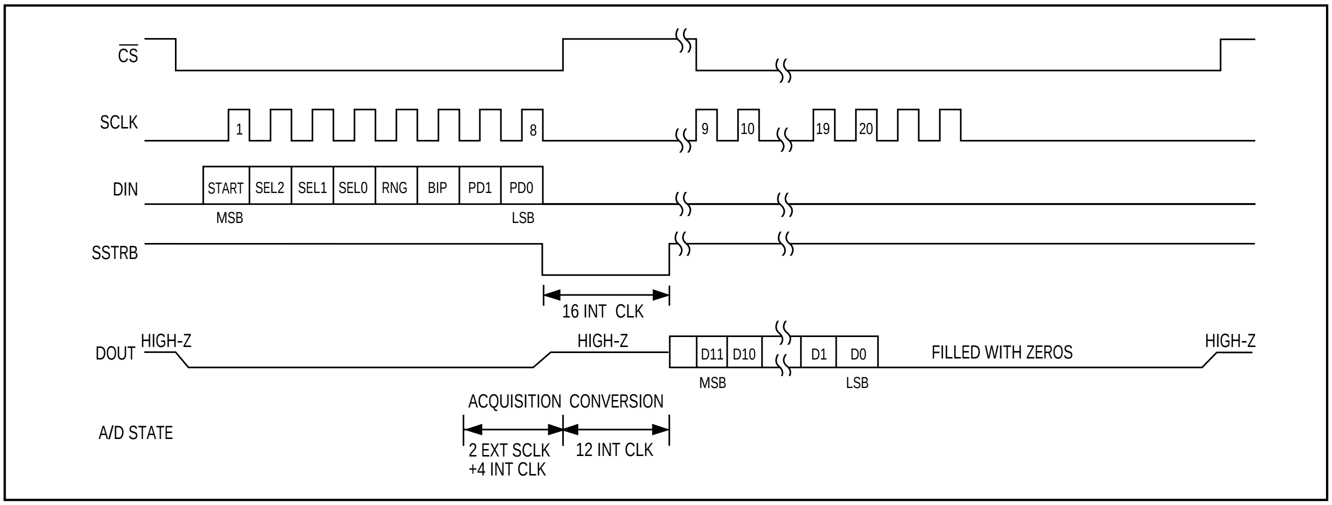


Figure 9. Internal Clock Mode—20 SCLK/Conversion Timing

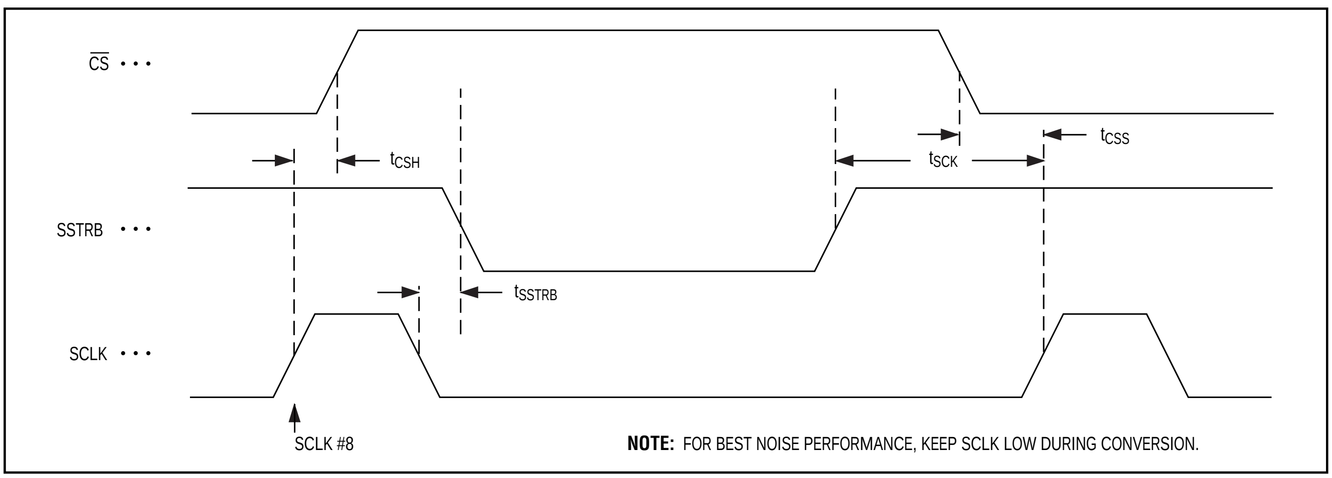


Figure 10. Internal Clock Mode—SSTRB Detailed Timing

conversion in progress. Figure 10 shows the SSTRB timing in internal clock mode.

Internal clock mode conversions can be completed with 13 external clocks per conversion but require a waiting period of 15µs for the conversion to be completed (Figure 11).

Most microcontrollers require that conversions occur in multiples of 8 SCLK clock cycles. Sixteen clock cycles per conversion (as shown in Figure 12) is typically the most convenient way for a microcontroller to drive the MAX1270/MAX1271.

Applications Information

Power-On Reset

The MAX1270/MAX1271 power up in normal operation (all internal circuitry active) and internal clock mode, waiting for a start bit. The contents of the output data register are cleared at power-up.

Internal or External Reference

The MAX1270/MAX1271 operate with either an internal or external reference. An external reference is connected to either REF or REFADJ (Figure 13). The REFADJ internal buffer gain is trimmed to 1.638V to provide 4.096V at REF from a 2.5V reference.

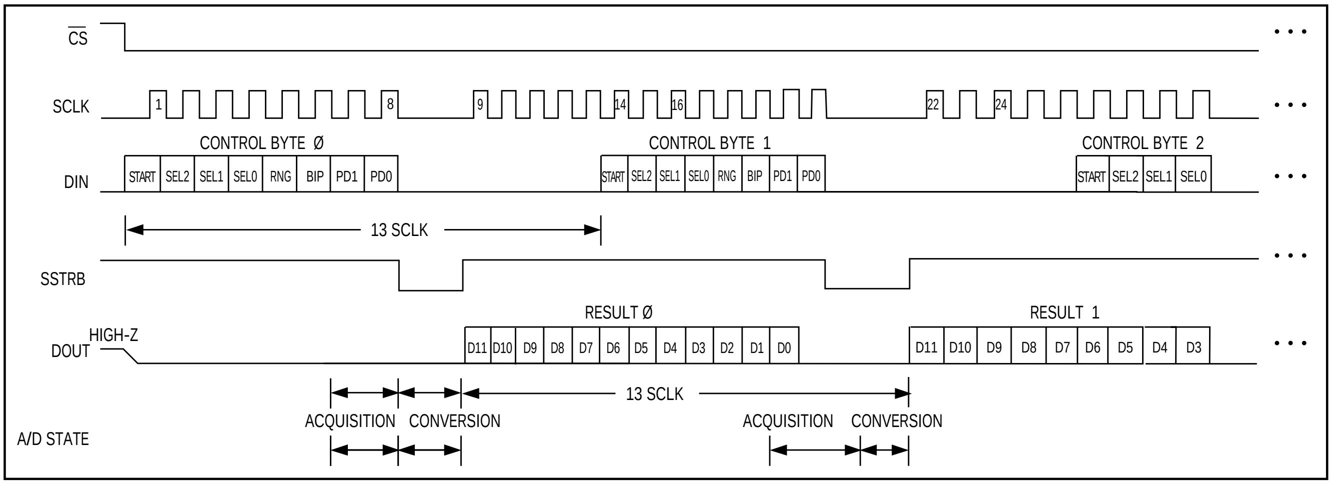


Figure 11. Internal Clock Mode—13 Clocks/Conversion Timing

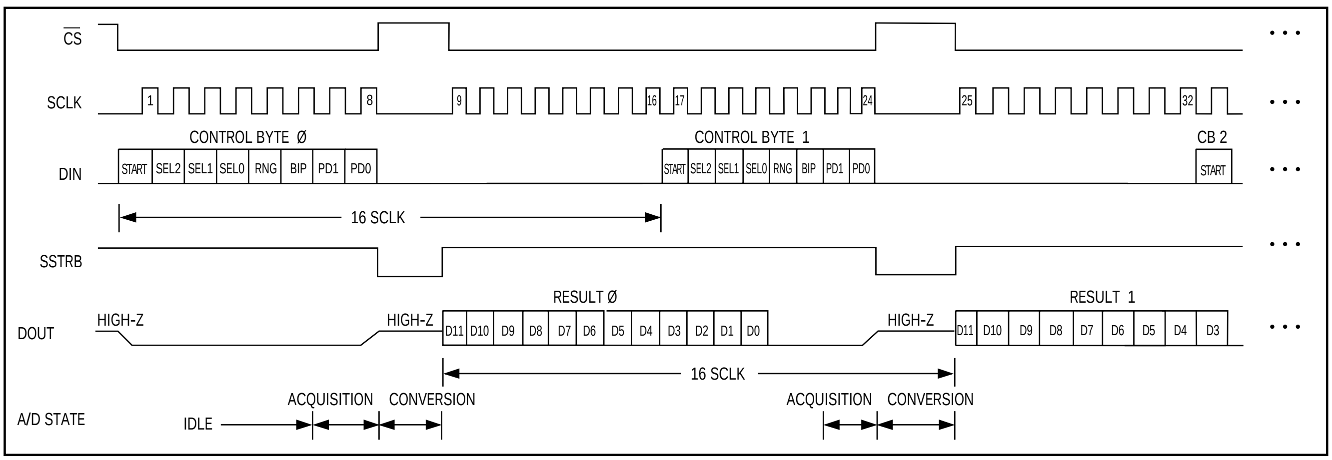


Figure 12. Internal Clock Mode—16 Clocks/Conversion Timing

Internal Reference

The internally trimmed 2.50V reference is amplified through the REFADJ buffer to provide 4.096V at REF. Bypass REF with a 4.7µF capacitor to AGND and REFADJ with a 0.01µF capacitor to AGND (Figure 13a). The internal reference voltage is adjustable to ±1.5% (±65 LSBs) with the reference-adjust circuit of Figure 1.

External Reference

To use the REF input directly, disable the internal buffer by tying REFADJ to V_{DD} (Figure 13b). Using the REFADJ input eliminates the need to buffer the reference externally. When a reference is applied at REFADJ, bypass REFADJ with a 0.01µF capacitor to AGND. Note that when an external reference is applied at REFADJ, the voltage at REF is given by:

$$V_{REF} = 1.6384 \times V_{REFADJ} \quad (2.4 < V_{REF} < 4.18)$$

(Figure 13c). At REF and REFADJ, the input impedance is a minimum of 10kΩ for DC currents. During conversions, an external reference at REF must be able to deliver 400µA DC load currents and must have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass REF with a 4.7µF capacitor to AGND as close to the chip as possible.

With an external reference voltage of less than 4.096V at REF or less than 2.5V at REFADJ, the increase in the ratio of RMS noise to the LSB value (full-scale / 4096) results in performance degradation (loss of effective bits).

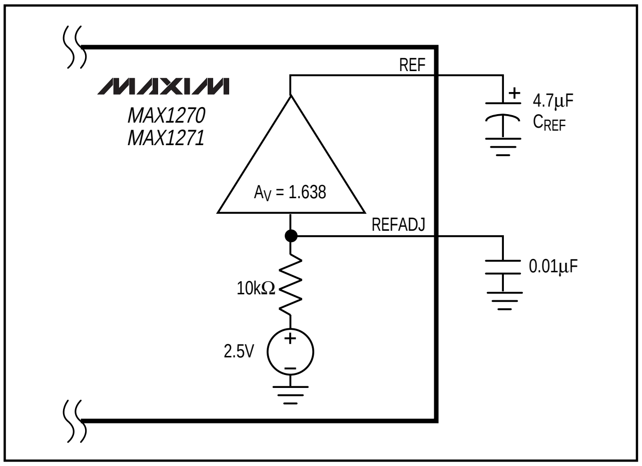


Figure 13a. Internal Reference

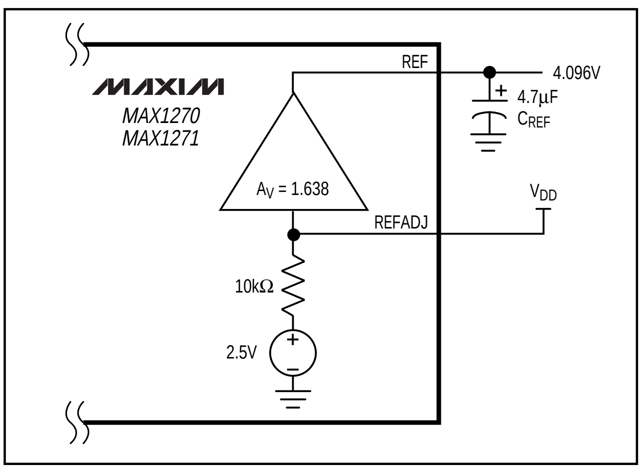


Figure 13b. External Reference—Reference at REF

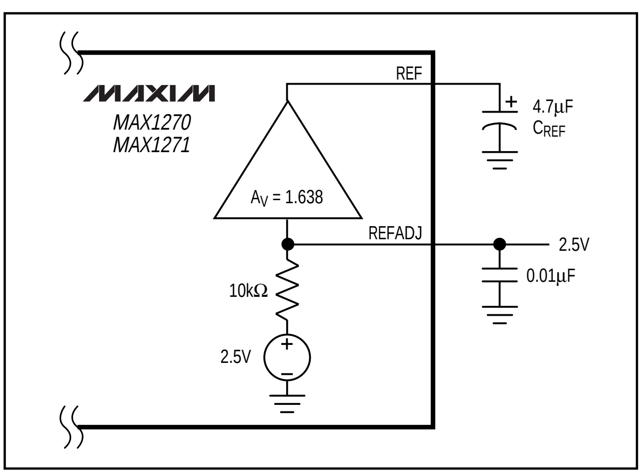


Figure 13c. External Reference—Reference at REFADJ

Power-Down Mode

To save power, configure the converter into low-current shutdown mode between conversions. Two programmable power-down modes are available in addition to a hardware shutdown. Select STBYPD or FULLPD by programming PD0 and PD1 in the input control byte (Table 4). When software power-down is asserted, it becomes effective only after the end of conversion. For example, if the control byte contains PD1 = 0, then the chip remains powered up. If PD1 = 1, then the chip powers down at the end of conversion. In all power-down modes, the interface remains active and conversion results can be read. Input overvoltage protection is active in all power-down modes.

The first logical 1 on DIN after $\overline{CS}$ falls is interpreted as a start condition, and powers up the MAX1270/MAX1271 from a software selected STBYPD or FULLPD condition.

For hardware-controlled power-down (FULLPD), pull SHDN low. When hardware shutdown is asserted, it becomes effective immediately, and any conversion in progress is aborted.

Choosing Power-Down Modes

The bandgap reference and reference buffer remain active in STBYPD mode, maintaining the voltage on the 4.7µF capacitor at REF. This is a DC state that does not degrade after power-down of any duration.

In FULLPD mode, only the bandgap reference is active. Connect a 33µF capacitor between REF and AGND to maintain the reference voltage between conversions and to reduce transients when the buffer is enabled and disabled. Throughput rates down to 1ksps can be achieved without allotting extra acquisition time for reference recovery prior to conversion. This allows conversion to begin immediately after power-up. If the discharge of the REF capacitor during FULLPD exceeds the desired limits for accuracy (less than a fraction of an LSB), run a STBYPD power-down cycle prior to starting conversions. Take into account that the reference buffer recharges the bypass capacitor at an 80mV/ms slew rate, and add 50µs for settling time.

Auto-Shutdown

Selecting STBYPD on every conversion automatically shuts down the MAX1270/MAX1271 after each conversion without requiring any start-up time on the next conversion.

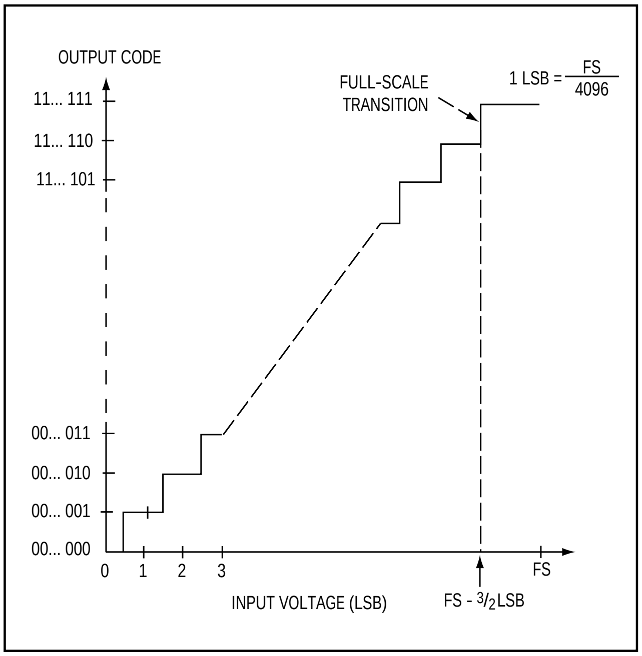


Figure 14a. Unipolar Transfer Function

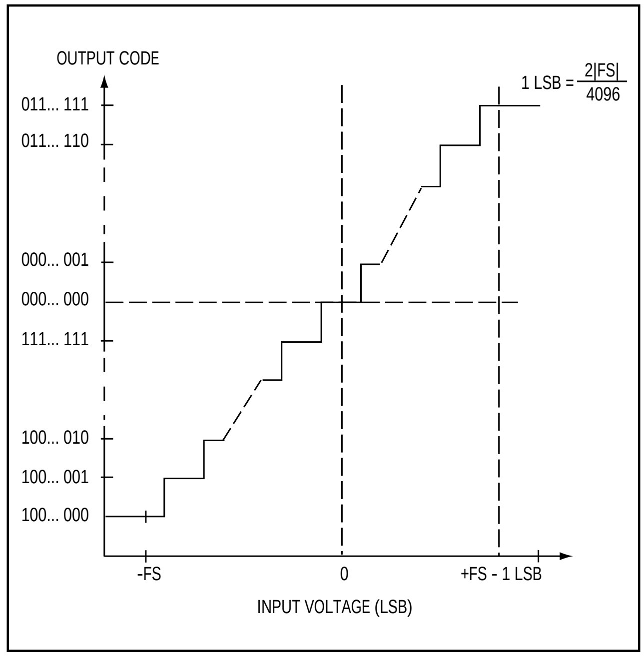


Figure 14b. Bipolar Transfer Function

Transfer Function

Output data coding for the MAX1270/MAX1271 is binary in unipolar mode with 1 LSB = (FS / 4096) and two's complement binary in bipolar mode with 1 LSB = [(2 x | FS |) / 4096]. Code transitions occur halfway between successive-integer LSB values. Figures 14a and 14b show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively. For full-scale values, refer to Table 3.

Layout, Grounding, and Bypassing

Careful PC board layout is essential for best system performance. Use a ground plane for best performance. To reduce crosstalk and noise injection, keep analog and digital signals separate. Connect analog grounds and DGND in a star configuration to AGND. For noise-free operation, ensure the ground return from AGND to the supply ground is low impedance and as short as possible. Connect the logic grounds directly to the supply ground. Bypass V_{DD} with 0.1µF and 4.7µF capacitors to AGND to minimize highand low-frequency fluctuations. If the supply is excessively noisy, connect a 5Ω resistor between the supply and V_{DD}, as shown in Figure 15.

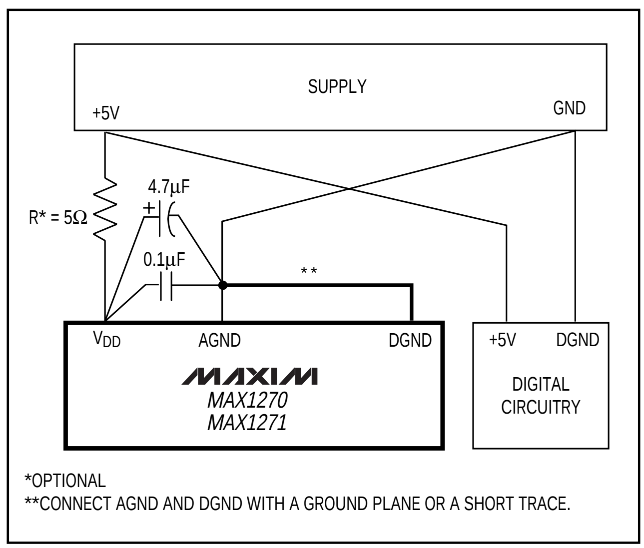
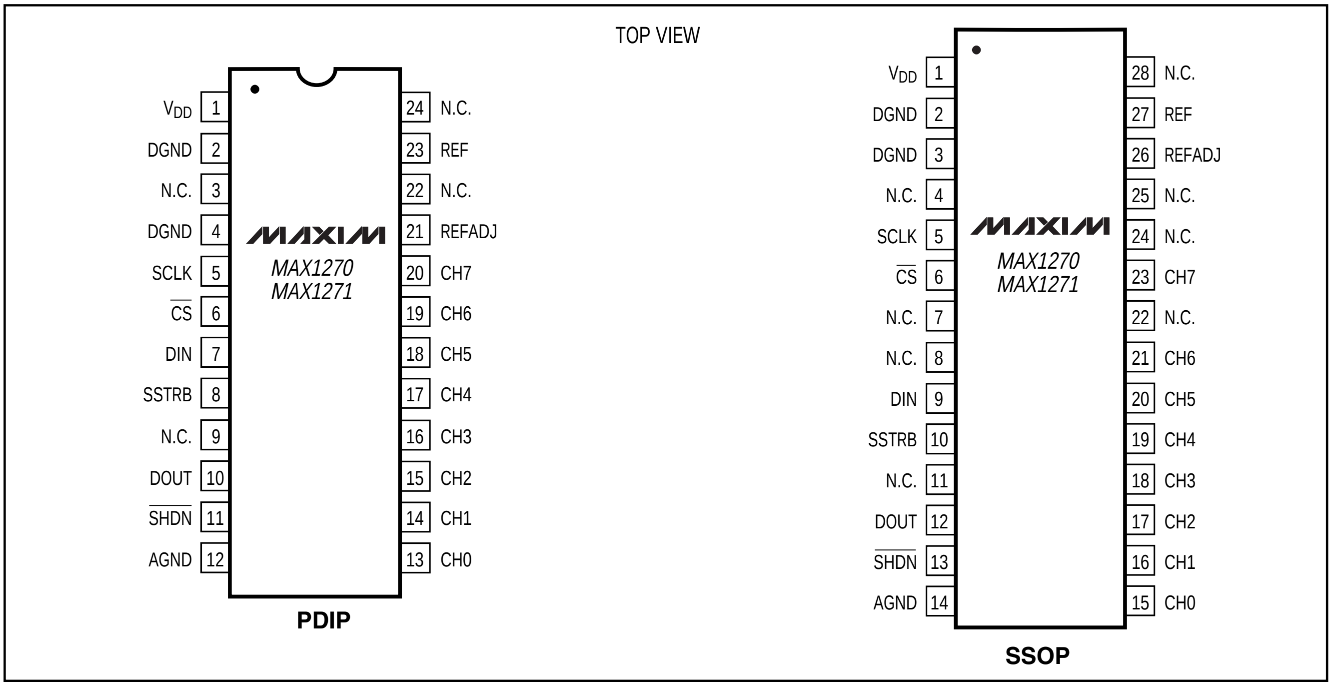


Figure 15. Power-Supply Grounding Connections

Pin Configurations



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX1270AENG	-40°C to +85°C	24 Narrow PDIP	±0.5
MAX1270BENG	-40°C to +85°C	24 Narrow PDIP	±1
MAX1270AEAI	-40°C to +85°C	28 SSOP	±0.5
MAX1270BEAI	-40°C to +85°C	28 SSOP	±1
MAX1271ACNG	0°C to +70°C	24 Narrow PDIP	±0.5
MAX1271BCNG	0°C to +70°C	24 Narrow PDIP	±1
MAX1271ACAI	0°C to +70°C	28 SSOP	±0.5
MAX1271BCAI	0°C to +70°C	28 SSOP	±1
MAX1271AENG	-40°C to +85°C	24 Narrow PDIP	±0.5
MAX1271BENG	-40°C to +85°C	24 Narrow PDIP	±1
MAX1271AEAI	-40°C to +85°C	28 SSOP	±0.5
MAX1271BEAI	-40°C to +85°C	28 SSOP	±1

Chip Information

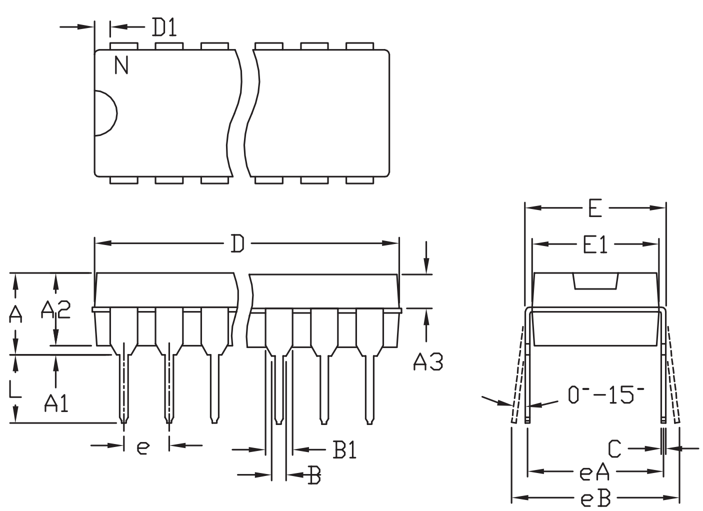
TRANSISTOR COUNT: 4219

SUBSTRATE CONNECTED TO AGND

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

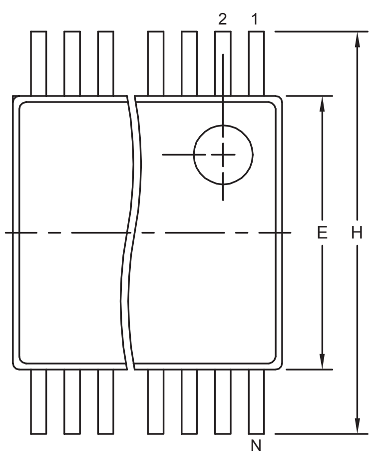
MAXIM 120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION	TITLE: PACKAGE FAMILY OUTLINE: PDIP .300"	1/1	DOCUMENT CONTROL NUMBER: 21-0043 REV: D

Multirange, +5V, 8-Channel, Serial 12-Bit ADCs

Package Information (continued)

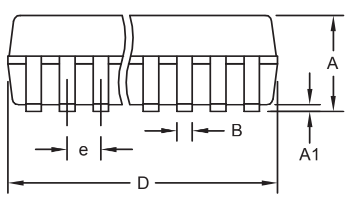
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

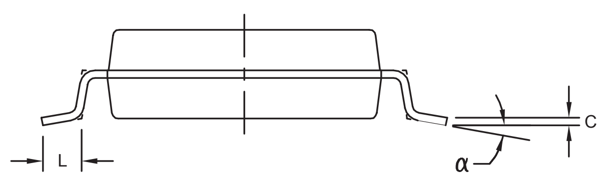
SSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0056 | REV. C | 1/1